WE CLAIM:

1. A bipolar junction transistor (BJT) fabricated with a process having a minimum process dimension of X μm, comprising:

a semi-insulating substrate,

a subcollector formed on said substrate,

a collector formed on said subcollector,

a first metal contact on said subcollector which provides a collector contact for said BJT,

a base formed on said collector,

an emitter formed on said base,

a cross-shaped second metal contact on said emitter which provides an emitter contact for said BJT, said emitter contact comprising two perpendicular arms which intersect at a central area, the width of each of said arms being about equal to X μm;

an inter-level dielectric layer on said emitter contact; and

a via through said inter-level dielectric layer which provides access to said emitter contact, said via being square-shaped, centered over the center point of said central area, and oriented at a 45° angle to said arms.

2. The BJT of claim 1, wherein said fabrication process has a minimum alignment tolerance, said square-shaped via sized as large as possible while maintaining said minimum alignment tolerance with respect to the boundaries of said emitter contact.

3. The BJT of claim 1, wherein said semi-insulating substrate comprises indium phosphide (InP).

4. The BJT of claim 1, wherein said semi-insulating substrate is a compound semiconductor.

5. The BJT of claim 1, wherein said arms are generally rectangular, have respective center points, are of approximately equal length, and intersect at their respective center points.

6. The BJT of claim 1, wherein said sub-collector comprises indium phosphide (InP) or indium gallium arsenide (InGaAs).

7. The BJT of claim 1, wherein said collector comprises indium phosphide (InP), indium gallium arsenide (InGaAs), indium aluminum arsenide (InAlAs), or indium aluminum arsenide phosphide (InAlAsP).

8. The BJT of claim 1, wherein said base comprises indium gallium arsenide (InGaAs).

9. The BJT of claim 1, wherein said base comprises gallium arsenide antimonide (GaAsSB).

10. The BJT of claim 1, wherein said emitter comprises indium phosphide (InP) or indium aluminum arsenide (InAlAs).

11. The BJT of claim 1, wherein said semi-insulating substrate is a compound semiconductor and said BJT structure is arranged to form a heterojunction bipolar transistor (HBT).

12. A heterojunction bipolar transistor (HBT) fabricated with a process having a minimum process dimension of X μm and a minimum alignment tolerance, comprising:

a semi-insulating substrate comprising a compound

semiconductor;

a subcollector formed on said substrate;

a collector formed on said subcollector;

a first metal contact on said subcollector which provides a collector contact for said HBT;

a base formed on said collector;

an emitter formed on said base;

a cross-shaped second metal contact on said emitter which provides an emitter contact for said BJT, said emitter contact comprising two perpendicular arms which intersect at a central area, the width of each of said arms being about equal to X μm;

an inter-level dielectric layer on said emitter contact; and

a via through said inter-level dielectric layer which provides access to said emitter contact, said via being square-shaped, centered over the center point of said central area, and oriented at a 45° angle to said arms, said square-shaped via sized as large as possible while maintaining said minimum alignment tolerance with respect to the boundaries of said emitter contact.

13. The HBT of claim 12, wherein said semi-insulating substrate comprises indium phosphide (InP).

14. The HBT of claim 12, wherein said arms are generally rectangular, have respective center points, are of approximately equal length, and intersect at their respective center points.

15. The HBT of claim 12, wherein said sub-collector comprises indium phosphide (InP) or indium gallium arsenide (InGaAs).

16. The HBT of claim 12, wherein said collector

comprises indium phosphide (InP), indium gallium arsenide (InGaAs), indium aluminum arsenide (InAlAs), or indium aluminum arsenide phosphide (InAlAsP).

17. The HBT of claim 12, wherein said base comprises indium gallium arsenide (InGaAs).

18. The HBT of claim 12, wherein said base comprises gallium arsenide antimonide (GaAsSb).

19. The HBT of claim 12, wherein said emitter comprises indium phosphide (InP) or indium aluminum arsenide (InAlAs).

20. A method of forming a bipolar junction transistor (BJT) with a fabrication process having a minimum process dimension of X μm and a minimum alignment tolerance, comprising:

providing a semi-insulating substrate,

depositing a layer of material suitable for use as a BJT subcollector on said substrate,

depositing a layer of material suitable for use as a BJT collector on said subcollector layer,

depositing a layer of material suitable for use as a BJT base on said collector layer,

depositing a layer of material suitable for use as a BJT emitter on said base layer,

depositing, patterning, and etching a first metal layer to provide an emitter contact for said BJT, said emitter contact being cross-shaped and comprising two perpendicular arms which intersect at a central area, the width of each of said arms being about equal to X μm;

patterning and etching said emitter layer to form an emitter below said emitter contact,

depositing, patterning, and etching a second

metal layer to provide a base contact for said BJT,

patterning and etching said base and collector layers to form a base and a collector,

depositing, patterning, and etching a third metal layer to provide a collector contact for said BJT,

patterning and etching said sub-collector layer to form a sub-collector below said collector,

depositing an inter-level dielectric layer on said emitter contact; and

patterning and etching a via through said inter-level dielectric layer which provides access to said emitter contact, said via being square-shaped, centered over the center point of said central area, and oriented at a 45° angle to said arms.

21. The method of claim 20, wherein said square-shaped via is sized as large as possible while maintaining said minimum alignment tolerance with respect to the boundaries of said emitter contact.

22. The method of claim 20, further comprising:

depositing a layer of material suitable for use as a BJT emitter cap on said emitter layer immediately after depositing said emitter layer, and

patterning and etching said emitter cap layer along with said emitter layer to form said emitter.

23. The method of claim 20, wherein said semi-insulating substrate comprises indium phosphide (InP).